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09/884,226	06/20/2001	Giovanni Traverso	Q65045	3000

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EXAMINER	
WONG, BLANCHE	

ART UNIT	PAPER NUMBER
2616	

DATE MAILED: 07/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/884,226	TRAVERSO ET AL.	
	Examiner	Art Unit	
	Blanche Wong	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-10 and 12-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-10 and 12-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The indicated allowability of claims 2-10 and 12-18 is withdrawn in view of the newly discovered reference Fourcade. Rejections based on the newly cited reference(s) is as follow.

Drawings

2. Examiner notes that replacement drawings are missing from the Amendment, dated May 30, 2006.

Claim Objections

3. Claim 2 is objected to because of the following informalities: Examiner suggests replacing "including" in line 2 with –comprising--. Appropriate correction is required.

4. Claim 16 is objected to because of the following informalities: Examiner suggests replacing "sampler of said delayed phase plurality" in lines 2-3 with "sampler of said plurality of delayed phases" in consistent with claim 15, line 3. Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. **Claims 2-10,12-18** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With regard to claim 2, it is unclear whether there is only one step of "measuring the phase ..." or there are more than one as indicated by the wording "including the steps..." in line 2.

With regard to claim 4, it is unclear what are "substantially" and "a sure data sequence" both in line 6. Similarly in claim 10.

With regard to claim 9, it is unclear what is meant by "provided at least one of the first two delayed phases or one of the last two delayed phases in at least one of the values sampled during the whole transit of the sure sequence" and what "differs from an aligned data flow".

With regard to claim 12, it is unclear what is "a sure data sequence" in lines 5-6. Similarly in claim 14.

With regard to claim 16, it is unclear whether there was a first enable signal given there is "a second enable signal" in line 3.

With regard to claim 16, it is unclear what is "the sure data sequence" in line 4.

With regard to claim 17, it is unclear what is "arranged downstream the sampler" in line 3.

7. There is insufficient antecedent basis for this limitation in the claim.

Claim 2 recites the limitation "said sure data sequence" in line 7.

Claim 6 recites the limitation "the sure data sequence" in line 3.

Claim 10 recites the limitation "the sure sequence" in lines 4-5.

Claim 14 recites the limitation "the masked clock signal" in line 3.

Claim 17 recites the limitation "the selection signals" in line 4.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. **Claims 2-10** are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Fourcade et al. (U.S. Pat No. 4,390,985).

With regard to claim 2, Fourcade discloses a method for aligning data flows in time division frames, comprising the steps of

measuring **(deriving and shaping circuit 14 in Fig. 1, col. 3, lines 38-40)** the phase of said input data flow **(Input E in Fig. 1, col. 3, line 8)** with respect to the phase of a reference signal **(clock 12 in Fig. 1, col. 3, lines 27 and 50)**, for controlling the delay time introduced by a delay line **(delay line 11 in Fig. 1, col. 3, line 29)** in said input data flow depending on the measured phase **(counter circuit 19 in Fig. 1, col. 3, line 66)**,

wherein the phase of the input data flow is measured in a time interval **(rhythm f based on rhythm F of clock 12)** corresponding to the transit time of a predefined data sequence **(reference signal, col. 3, line 49 and 62; see also output of multiplexer 18 in Fig. 1)** comprised in said input flow **("comparing the possible transmissions of the input bits with the signals displaced relative to one another by 1/kf obtained**

from a clock of rhythm F=kf', col. 3, lines 14-16; and "The output of clock is connected to the input of a divider by k circuit supplying on k outputs signals of rhythm f displaced in time with respect to one another by a fast clock signal cycle of rhythm F", col. 3, lines 49-53), and

wherein the flow of said sure data sequence **(reference signal)** containing a logic transition **(divider 17 and multiplexer 18 in Fig. 1)** is detected **(input D of D flip-flips 15,16,25,26 in Fig. 1)**, and consequently an enable signal **(output Q of D flip-flops 15,16,25,26 in Fig. 1; see also sampling control input to the sampling circuit 13 in Fig. 1, col. 3, lines 31-32)** activating a phase sampling operation **(sampling circuit 13 in Fig. 1, col. 3, line 31)** is generated.

With regard to claim 3, Fourcade further discloses a masked reference signal **(rhythm f of F)** that is obtained from a reference signal **(clock)**.

With regard to claim 4, see analysis for claim 2. Fourcade further discloses a delay line **(delay line 11 in Fig. 1, line 3, line 10)** that is provided with a fixed delay for producing a plurality of delayed phases from an input data flow **(a shift register having a shift clock input, col. 3, lines 10-11)**.

With regard to claim 5, Fourcade further discloses a masked reference signal **(rhythm f of F)** that is used for controlling execution of a sampling operation **(sampling circuit 13)** of a plurality of delayed phases.

With regard to claim 6, Fourcade further discloses a second enable signal **(sampling control input to the sampling circuit 13)** that is obtained indicating the presence of the logic transition **(counter circuit 19)**, and said second enable signal is used for activating the sampling operation **(sampling circuit 13)** of a said plurality of delayed phases.

With regard to claim 7, Fourcade discloses the method according to claim 6. XXX discloses a second enable signal **(sampling control input to the sampling circuit 13)** that is obtained from a correction signal **(output from multiplexer 28 in Fig. 1)** deriving from an alignment operation **(counter circuit 19 + memory register 27 + multiplexer 28)** of an input data flow **(Input E)**.

With regard to claim 8, Fourcade discloses a result of a sampling operation **(sampling circuit 10 in Fig. 1)** that is supplied to a control logic **(delay line 11 in Fig. 1)**, which generates selection for controlling the delay time of a delay line **(delay line)**, depending on the result of the sampling operation.

With regard to claim 9, Fourcade discloses a control logic **(counter circuit 19 in Fig. 1)** that decides for incrementing or decrementing **(forwarding counting input and backward counting input, col. 3,lines 67-68)** by one the index i of the selection signals.

With regard to claim 10, see analysis for claim 2.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. **Claims 12-17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fourcade in view of Farwell (U.S. Pat No. 5,870,445).

With regard to claim 12, Fourcade discloses a phase alignment circuit of an input data flow, comprising:

a phase equalizer **(Fig. 1)** for equalizing the phase of a reference signal **(clock 12)** with the phase of the input data flow **(Input E)** and driving, through appropriate selection signals **(output Q of D flip-flips 15,16,25,26)**, a delay line **(delay line 11)** operating on the input data flow **(Input E)**, wherein a detector **(counter circuit 19)** is provided for the transit of a sure data sequence **(reference signal, col. 3, line 49 and 62; see also output of multiplexer 18 in Fig. 1)** containing a logic transition comprised in the input data flow, wherein said detector controls the operation of the phase equalizer through an enable signal **(output Q of D flip-flips 15,16,25,26; see also sampling control input to the sampling circuit 13) (see also analysis for claim 2)**.

However, Fourcade fails to explicitly show a variable delay line.

In an analogous art, Farwell discloses a variable delay line **(variable delay line, col. 3, line 17; see also Fig. 3)**.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include a variable delay line in Fourcade's phase alignment circuit. The suggestion/motivation for doing so would have been to provide for freedom from discontinuities. Farwell, col. 1, line 61. Therefore, it would have been obvious to combine Farwell with Fourcade for the benefit of a variable delay line, to obtain the invention as specified in claim 12.

With regard to claim 13, the combination of Fourcade and Farwell discloses a phase alignment circuit according to claim 12. Fourcade further discloses a logic masker **(divider 17 + multiplexer 18 + D flip-flops 15,16,25,26 + counter circuit 19)** that is provided from obtaining a masked clock signal **(output of counter circuit 19 in Fig. 1)** from the combination of the enable signal **(output Q of D flip-flips 15,16,25,26)** and reference signal **(clock)**.

With regard to claim 14, see analysis for claim 12.

Farwell further discloses a delay line which produces a plurality of delayed phases **(Q outputs of an N-stage bidirectional shift register, col. 3, line 48-49)**.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include a delay line which produces a plurality of delayed phases in the combination of Fourcade and Farwell. The suggestion/motivation for doing so would have been to provide for freedom from discontinuities. Farwell, col. 1, line 61. Therefore, it would have been obvious to combine a delay line which produces a plurality of delayed phases with the combination of Fourcade and Farwell for the benefit of a delay line which produces a plurality of delayed phases, to obtain the invention as specified in claim 14.

With regard to claim 15, the combination of Fourcade and Farwell discloses a phase alignment circuit according to claim 14. Fourcade further discloses a sampler **(sampling circuit 13)** of a plurality of delayed phases, which employ a masked clock signal **(output of counter circuit 19 in Fig. 1)** as a clock signal.

With regard to claim 16, the combination of Fourcade and Farwell discloses a phase alignment circuit according to claim 15. Fourcade further discloses a sampler **(sampling circuit 13)** of a plurality of delayed phases that receives at least a second enable signal **(sampling control input to the sampling circuit 13)** generated by the detector **(counter circuit 19)**, which indicates the transit of the transition in the sure data sequence **(reference signal, col. 3, line 49 and 62; see also output of multiplexer 18 in Fig. 1)**.

With regard to claim 17, the combination of Fourcade and Farwell discloses a phase alignment circuit according to claim 15. Fourcade further discloses a control logic **(sampling circuit 13)** for receiving the sampled values of a plurality of delayed phases and emitting selection signals depending on them.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Blanche Wong whose telephone number is 571-272-3177. The examiner can normally be reached on Monday through Friday, 830am to 530pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on 571-272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BW
July 12, 2006

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